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| EXAMINER | |
|---|---|
| HARKNESS, CHARLES A | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | 9 |

DATE MAILED: 06/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/745,549 | SAGER ET AL. | |
| | Examiner | Art Unit | |
| | Charles A Harkness | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *22 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *8-24 and 28-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-24 and 28-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. In view of the amendment to the title, the objection to the specification has been withdrawn.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 8-13, 15-24, and 28-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Blomgren et al., U.S. Patent Number 6,334,183 (herein referred to as Blomgren).

3. Referring to claims 11 and 34 Blomgren has taught a method for sub-register data operations for executing an instruction, the method comprising:

executing the instruction on a first register and a second register;

disabling a carryover of a result of the executed instruction from low-order bit positions of a result register to the high-order bit positions of the result register (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10; since the bits that are not involved in the addition are filled by the source registers previous value, the carryover bit is left out of the register when a value is passed through; however, when all of the bits of the operands are being added, a carry bit would be carried over the carry line from the each of the LOW and HIGH adders go on to the TOP adder, with the LOW's carry also going to the HIGH adder – this is required when adding all of the bits of the operands together to calculate the correct value. - the carryover bit would

only be disabled when the values are passed through to the result register, as shown in the table in figure 2);

and merging a result of the executed instruction with a plurality of high-order bits from the first register, the plurality of high-order bits being copied into high-order bit positions from the first register, the plurality of high-order bits being copied into high-order bit positions of a result register, and the result being placed into low-order bit positions of the result register (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10; as shown in figure 2, when the add BX,AX->AX instruction is executed, the unchanged portion of the register is passed though while the result of the lower portion of the registers is calculated).

4. Referring to claims 8 and 35 Blomgren has taught wherein the merging a result comprises: modifying contents of the second register by placing data values of zero in the high-order bit positions of the second register; adding contents of the first register with the modified second register; and placing the result in the result register (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10).

5. Referring to claims 9 and 36 Blomgren has taught the method further comprising: ignoring a carryover of the result from the low-order bit positions of the result register to the high-order bit positions of the result register (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10; since the bits that are not involved in the addition are filled by the source registers previous value, the carryover bit is left out of the register).

6. Referring to claims 10 and 37 Blomgren has taught wherein the merging a result comprising: modifying contents of the first register by placing data values of zero in the low-order bit positions of the first register; modifying contents of the second register by placing data

values of zero in the high-order bit positions of the second register; adding the modified first register with the modified second register; and placing the result in the result register (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10; as shown in figure 2, when the instruction ADD BL,AH->AH the lower portion of B is added to the middle portion of A, which results in the counterparts being zeroed).

7. Referring to claim 12 Blomgren has taught wherein the first register and the second register have 32 bits (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10).

8. Referring to claim 13 Blomgren has taught wherein the result register has 32 bits (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10).

9. Referring to claim 15 Blomgren has taught wherein the result of the executed instruction is less than 32 bits (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10).

10. Referring to claim 16 Blomgren has taught wherein the result of the executed instruction is less than or equal to 16 bits (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10).

11. Referring to claim 17 Blomgren has taught wherein the result of the executed instruction is less than or equal to 8 bits (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10).

12. Referring to claim 18 Blomgren has taught wherein the merging a result is performed before instruction execution is complete (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10; the result and the unchanged portion of the register are available to the destination register at the same time).

13. Referring to claim 19 Blomgren has taught a processor comprising: an instruction set having an instruction; a source register and a destination register referenced by the instruction from the instruction set; and a logic circuit to examine the instruction before execution to

identify a portion of the source register that should remain unchanged into the destination register, and the logic circuit further to move the unchanged portion into the destination register before instruction execution is complete (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10; as shown in figure 2, when the add BX,AX->AX instruction is executed, the unchanged portion of the register is passed though while the result of the lower portion of the registers is calculated).

The logic circuit including a carryover circuit to disable a carryover from the execution of the instruction to the unchanged portion of the destination register (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10; since the bits that are not involved in the addition are filled by the source registers previous value, the carryover bit is left out of the register when a value is passed through; however, when all of the bits of the operands are being added, a carry bit would be carried over the carry line from the each of the LOW and HIGH adders go on to the TOP adder, with the LOW's carry also going to the HIGH adder – this is required when adding all of the bits of the operands together to calculate the correct value. - the carryover bit would only be disabled when the values are passed through to the result register, as shown in the table in figure 2).

14. Referring to claim 20 Blomgren has taught wherein the logic circuit is to move the unchanged portion into the destination register by setting corresponding values of the source register to zero (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10).

15. Referring to claim 21 Blomgren has taught wherein the source register and the destination register have a greater bit-length than a result of the instruction (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10).

16. Referring to claim 22 Blomgren has taught wherein the source register and the destination register have 32 bits (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10).

17. Referring to claim 23 Blomgren has taught wherein the result of the instruction has less than 32 bits (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10).

18. Referring to claim 24 Blomgren has taught wherein the result of the instruction is less than or equal to 16 bits (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10).

19. Referring to claims 28 and 31 Blomgren has taught a method comprising:

receiving an instruction to perform an operation on contents of first and second source registers, the contents including a plurality of bits and the operation results being a different bit length then bit lengths of the first and second source registers (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10; as shown in figure 2, and in the specification, the result of 8 bits is smaller than the 32 bit registers);

identifying high order bits of one of the source registers that should remain unchanged when merged into the destination register; and

modifying the contents of the other source register by setting corresponding high order bits of the other source register to zero (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10; as shown in figure 2, when the add BX,AX->AX instruction is executed, the unchanged portion of the register is passed though while the result of the lower portion of the registers is calculated);

adding the contents of the one of the source registers with the modified contents of the other source register; and

placing results of the addition in the destination register (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10).

disabling a carryover of the addition results from low-order bit positions of the destination register to high-order bit positions of the destination register (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10; since the bits that are not involved in the addition are filled by the source registers previous value, the carryover bit is left out of the register when a value is passed through; however, when all of the bits of the operands are being added, a carry bit would be carried over the carry line from the each of the LOW and HIGH adders go on to the TOP adder, with the LOW's carry also going to the HIGH adder – this is required when adding all of the bits of the operands together to calculate the correct value. - the carryover bit would only be disabled when the values are passed through to the result register, as shown in the table in figure 2).

20. Referring to claims 29 and 32 Blomgren has taught wherein screening the first and second source registers comprising: modifying contents of one of the source register by setting low order bits of the one of the source registers to zero; and modifying the contents of the other source register by setting high order bits of the other source register to zero (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10; as shown in figure 2, when the instruction ADD BL,AH->AH the lower portion of B is added to the middle portion of A, which results in the counterparts being zeroed).

21. Referring to claims 30 and 33 Blomgren has taught wherein merging the operation results comprising: adding the modified contents of the one of the source registers with the modified

contents of the other source; and placing results of the addition into the destination register (Blomgren abstract, figure 2, column 9 line 64-column 10 line 10).

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blomgren in view of Zuraski, Jr. et al, U.S. Patent Number 5737629 (herein referred to as Zuraski).

23. Referring to claim 14 Blomgren has not taught the method further comprising: using a renamer to assign the first register, the second register, and the result register. Zuraski has taught the method further comprising: using a renamer to assign the first register, the second register, and the result register (Zuraski column 2 lines 23-29, column 11 lines 21-33, figure 13). Zuraski has shown that renaming registers, or partial registers, prevents certain instructions from being dependent on each other, which would stall the execution of the dependent instruction. Thus, by renaming the partial registers, reduces the amount of stalls that occur from data dependency and thus reduces the amount of time required for execution. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to rename registers to reduce the amount of time required for exaction.

### *Response to Arguments*

24. Applicant's arguments filed 1/20/04, paper number 7, have been fully considered but they are not persuasive.

25. In the remarks, in regard to the rejection of claim 1, Applicant argues in essence that:

> "There is nothing in the Blomgren et al. patent that discloses or suggests 'disabling a carryover of a result of the executed instruction from low-order bit positions of the result register to high-order bit positions of the result register,' as recited in claim 11."

26. This is not found persuasive. Looking at figure 2, one of ordinary skill in the art at the time of the invention would recognize that a carry line from the each of the LOW and HIGH adders go on to the TOP adder, with the LOW's carry also going to the HIGH adder. One would recognize that when adding either the entire A and B operands together or adding 15:0 bits of the two operands, carry bits would have to be passed to the adder of the next significant bits so that the correct value would be computer. The carryover bit would only be disabled when the values are passed through to the result register, as shown in the table in figure 2.

## *Conclusion*

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 703-305-7579. The examiner can normally be reached on 8:00 A.M. – 5:30 P.M. with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-7579.

Charles Allen Harkness

Patent Examiner

Art Unit 2183

May 27, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
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